# ML610413P/ML610Q413P **Preliminary**

8-bit Microcontroller with a Built-in LCD driver

## GENERAL DESCRIPTION

ML610413P is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as Real Time Clock, Random Number Generator, Watch Dog Timer, 16bit Timer, Synchronous Serial port,, Security Mesh, and LCD driver, are incorporated around OKI SEMICONDUCTOR's original 8-bit CPU nX-U8/100. The CPU nX-U8/100 is capable of efficient instruction execution in one clock with 3-stage pipelined processing. The ML610413P operates in both high and low-speed mode and has power-saving modes. It is designed specifically for battery operated products.

## FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Minimum instruction execution time
    30.5 µs (@32.768 kHz system clock)
    2µs (@500kHz system clock)
    0.244µs (@4.096 MHz system clock)

- Internal memory
  ML610413P:
    - Internal 16KByte Mask ROM (8K×16 bits)
    - Internal 512Byte Data RAM (512×8 bits)

  ML610Q413P:
    - Internal 16KByte FLASH ROM (8K×16 bits)
    - Internal 512Byte Data RAM (512×8 bits)

- Interrupt controller
  - 3 non-maskable interrupt sources
    Internal source: 2 (Security Mesh, Watch dog timer),
    External source: 1 (NMI)
  - 14 maskable interrupt sources
    Internal sources: 6 (SSIO0, Timer0, Timer1, RTC, Alarm0, Alarm1)
    External sources: 8 (P00, P01, P02, P03, P04, P05, P06, P07)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. –488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Real time clock
  - Year, month, day, day of the week, hour, minute, and second registers
  - Adjustable to compensate for crystal variations
  - Automatic leap year correction
  - Regular interrupts (0.5 sec, 1 sec, 1 minute)
  - Alarm interrupt × 2 channels (day of the week, hour, minute; month, day, hour, minute)

- Random Number Generator
  - Deterministic random number generation which has passed NIST800-22 test
  - Pre-process based Seed generation by modified Linear Feedback Shift Register and post-process by AES
  - AES stand-alone mode which can execute only AES
    Plaintext/ciphertext size: 128bits
    Key size: 128bits
    ECB mode

- Watchdog timer
  - Non-maskable interrupt generated by the first overflow and reset generated by the second overflow
  - Start by writing to the control register and can not be turned off by software or external input
  - One of four types of overflow periods (125ms, 500ms, 2s, and 8s) selectable

- Timers
  - 8 bits × 2 channels (16-bit × 1 configuration available)

- Capture
  - 8 bit time base capture × 2 channels (4096 Hz to 32 Hz)

- Synchronous serial port
  - Master/slave selectable × 1 channel
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable
  - SPI operating in mode 0/3
  - Overflow detection

- General-purpose ports
  - Output-only port
    2 channels (including secondary functions)
  - Input/output port × 20 channels (including secondary functions)

- LCD driver
  - Max. 80 segments (20seg×4com, 20seg×3com, and 20seg×2com selectable)
  - 1/1 to 1/4 duty
  - 1/2, 1/3 bias (built-in bias generation circuit)
  - Frame frequency selectable: approx. 16Hz, 64Hz, 73Hz, and 85Hz
  - Bias voltage multiplying clock selectable (8 types)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the second watchdog timer (WDT) overflow
  - Software reset by execution of the BRK instruction
  - Security Mesh reset by detecting the cut of the top metal line

  Note: Power-On-Reset (POR) built internally. All resets ( except POR and the Security Mesh reset ) leave the contents of RAM and of certain peripheral registers unchanged except CPU. No registers would be affected by a reset ( except POR and Security Mesh reset ). The POR and the Security Mesh reset initialize all registers ( except for the Reset Status Register ).

- Clock
  - Low-speed clock: Crystal oscillation (32.768 kHz)
    (This LSI can not guarantee the operation without low-speed crystal oscillation clock)
  - High-speed clock: Built-in RC oscillation (500 kHz, typ.+/ –10%), Built-in PLL oscillation (8.192MHz)
  - Start operation with the low-speed clock
  - Selection of high-speed clock mode by software:
    RC oscillation, built-in PLL oscillation
  - Output clock:
    Low-speed output clock
    High-speed output clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - High-speed Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8 of the oscillation clock)
  - Block Control Function: Resets and completely turns circuits of unused peripherals off.

- Security Mesh
  - Covered with the metal line to prevent to have the internal signal tampered or probed
  - Start by writing to the control register and can not be turned off by software.
  - When detected the cut of the top metal line, the non-maskable interrupt , the reset selectable.
  - When selected the reset and detected the cut of the top metal line, the Security Mesh changes all RAM to 00H and initializes all registers(except for the Reset Status Register).

- Shipment
  - MASK ROM version: Die
    ML610413P-xxxWA
  - MASK ROM version: 64pin plastic TQFP
    ML610413P-xxxTB
  - MASK ROM version: 64pin plastic TFBGA
    ML610413P-xxxLA
  - FLASH ROM version: 64pin plastic TQFP
    ML610Q413P-NNNTB

  xxx: ROM code number
  WA: Die
  TB: TQFP (P-TQFP64-1010-0.50-ZK1)
  LA: TFBGA (P-TFBGA64-0606-0.50)

- Operating Conditions
  - Operating temperature: –40°C to +85°C
  - Operating voltage: $V_{DD}$ = 2.4V to 3.6V

## BLOCK DIAGRAM

### ML610413P Block Diagram

Figure 1 shows the block diagram of the ML610413P.
"*" indicates the secondary function of each port.

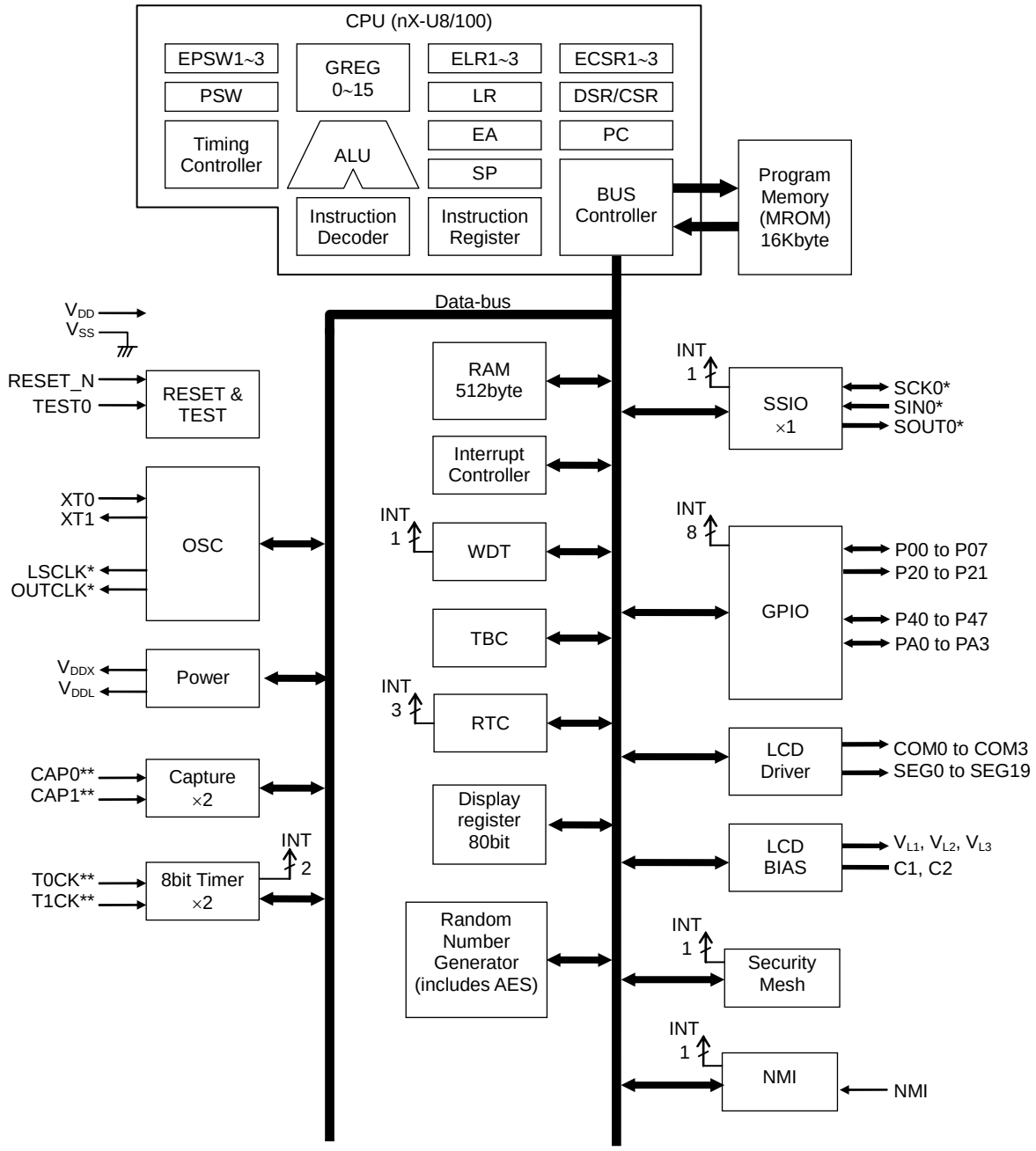



**Figure 1 ML610413P Block Diagram**

### ML610Q413P Block Diagram

Figure 2 shows the block diagram of the ML610Q413P.
"*" indicates the secondary function of each port.

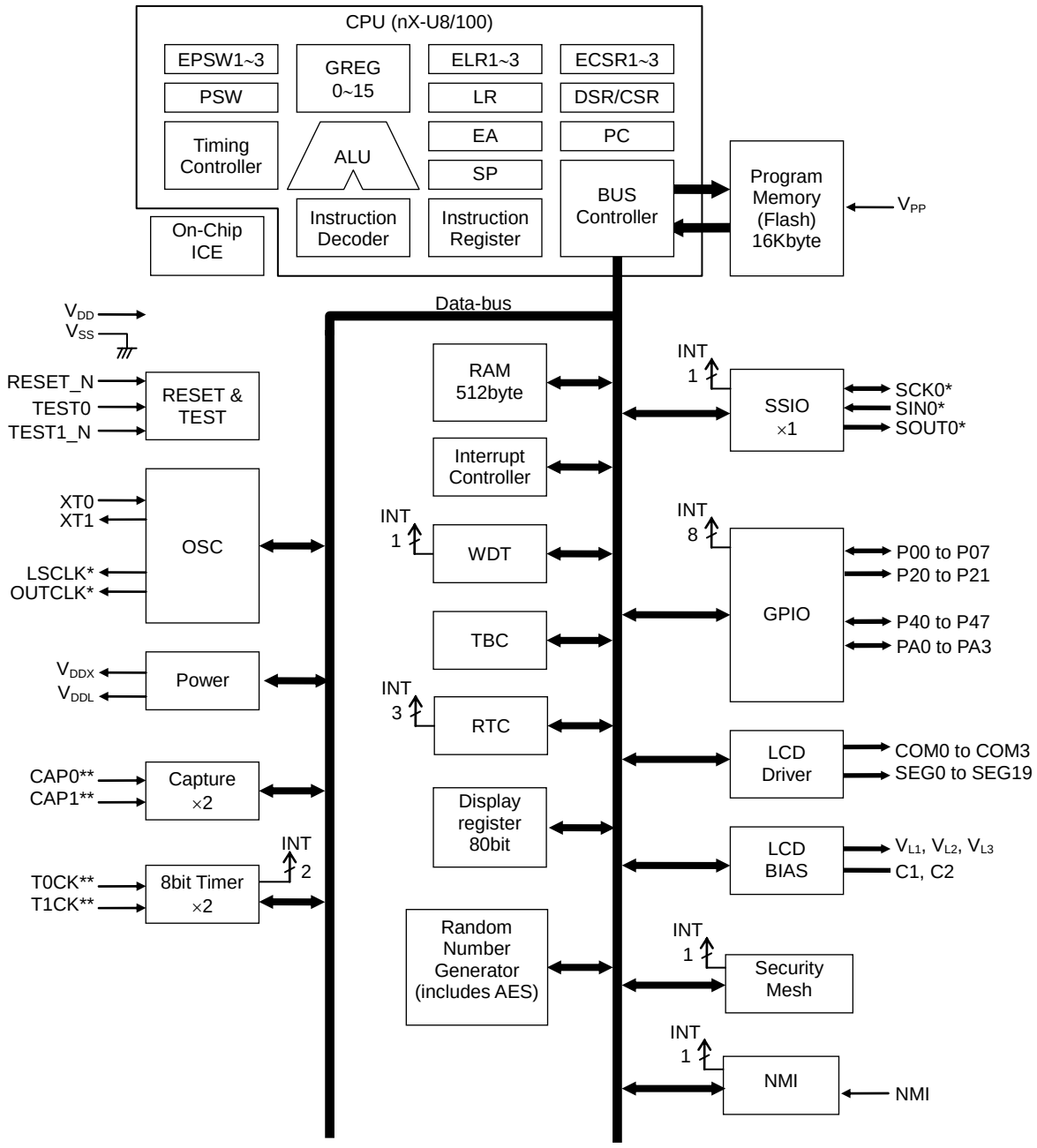
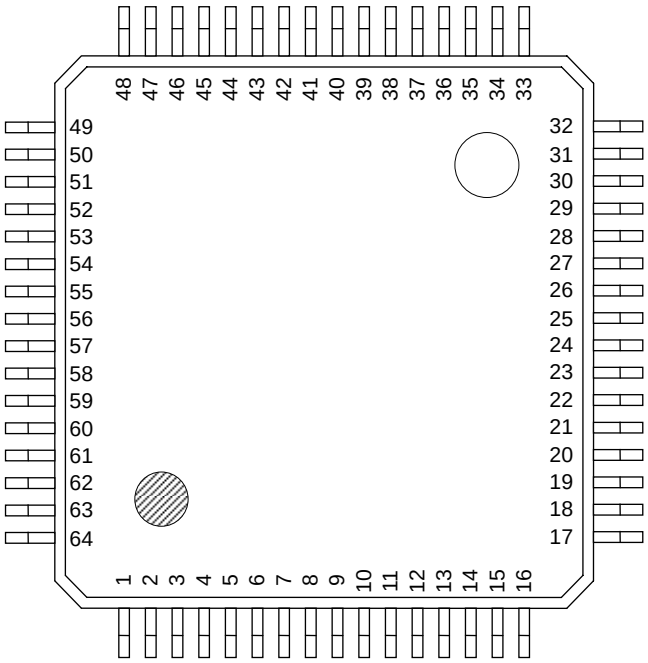



**Figure 2 ML610Q413P Block Diagram**

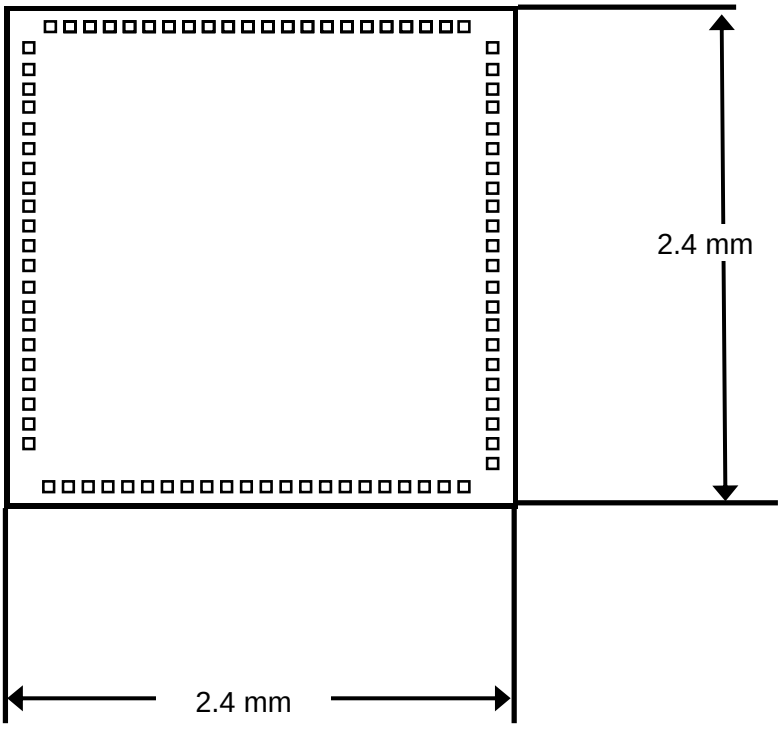
**ML610413P/ML610Q413P TQFP Package Pin Layout**




(NC): No Connection

**Figure 3 ML610413P/ML610Q413P TQFP Package Pin Layout**

**ML610413P Chip Pin Layout & Dimension**




| | |
|---|---|
| Chip size: | 2.4 mm × 2.4 mm |
| PAD count: | 64 |
| Minimum PAD pitch: | 80 μm |
| PAD aperture: | 70 μm × 80 μm |
| Chip thickness: | 350 μm |
| Voltage of the rear side of chip: | $V_{SS}$ level |

**Figure 4 ML610413P Chip Pin Layout & Dimension**

**ML610413P Pad Coordinates (TBD)**

**Table 1 ML610413P Pad Coordinates**

Chip Center: X=0,Y=0

| PAD No. | Pad Name | ML610413P | |
|---|---|---|---|
| | | X (µm) | Y (µm) |
| 1 | P06 | | |
| 2 | P07 | | |
| 3 | PA0 | | |
| 4 | PA1 | | |
| 5 | PA2 | | |
| 6 | PA3 | | |
| 7 | NMI | | |
| 8 | VDD | | |
| 9 | VSS | | |
| 10 | VDDL | | |
| 11 | VDDX | | |
| 12 | XT0 | | |
| 13 | XT1 | | |
| 14 | RESET_N | | |
| 15 | TEST0 | | |
| 16 | — | | |
| 17 | C1 | | |
| 18 | C2 | | |
| 19 | VL1 | | |
| 20 | VL2 | | |
| 21 | VL3 | | |
| 22 | NC | | |
| 23 | COM0 | | |
| 24 | COM1 | | |
| 25 | COM2 | | |
| 26 | COM3 | | |
| 27 | SEG0 | | |
| 28 | SEG1 | | |
| 29 | SEG2 | | |
| 30 | SEG3 | | |
| 31 | SEG4 | | |
| 32 | SEG5 | | |
| 33 | SEG6 | | |
| 34 | SEG7 | | |
| 35 | SEG8 | | |
| 36 | SEG9 | | |
| 37 | SEG10 | | |
| 38 | SEG11 | | |
| 39 | SEG12 | | |
| 40 | SEG13 | | |
| 41 | SEG14 | | |
| 42 | SEG15 | | |
| 43 | SEG16 | | |
| 44 | SEG17 | | |
| 45 | SEG18 | | |
| 46 | SEG19 | | |
| 47 | VSS | | |
| 48 | — | | |

| PAD No. | Pad Name | ML610413P | |
|---|---|---|---|
| | | X (µm) | Y (µm) |
| 49 | P20 | | |
| 50 | P21 | | |
| 51 | P40 | | |
| 52 | P41 | | |
| 53 | P42 | | |
| 54 | P43 | | |
| 55 | P44 | | |
| 56 | P45 | | |
| 57 | P46 | | |
| 58 | P47 | | |
| 59 | P00 | | |
| 60 | P01 | | |
| 61 | P02 | | |
| 62 | P03 | | |
| 63 | P04 | | |
| 64 | P05 | | |

**PIN LIST**

| PIN No. | Primary function | | | Secondary function | | | |
|---|---|---|---|---|---|---|---|
| | Pin name | I/O | Function | Secondary | Pin name | I/O | Function |
| 9,47 | $V_{SS}$ | — | Negative power supply pin | — | — | — | — |
| 8 | $V_{DD}$ | — | Positive power supply pin | — | — | — | — |
| 10 | $V_{DDL}$ | — | Power supply pin for internal logic (internally generated) | — | — | — | — |
| 11 | $V_{DDX}$ | — | Power supply pin for low-speed oscillation (internally generated) | — | — | — | — |
| 48 | $V_{PP}$(*1) | — | Power supply pin for Flash ROM | — | — | — | — |
| 19 | $V_{L1}$ | — | Power supply pin for LCD bias (internally generated or connected positive power supply pin) | — | — | — | — |
| 20 | $V_{L2}$ | — | Power supply pin for LCD bias (internally generated or connected positive power supply pin) | — | — | — | — |
| 21 | $V_{L3}$ | — | Power supply pin for LCD bias (internally generated or connected positive power supply pin) | — | — | — | — |
| 17 | C1 | — | Capacitor connection pin for LCD bias generation | — | — | — | — |
| 18 | C2 | — | Capacitor connection pin for LCD bias generation | — | — | — | — |
| 15 | TEST0 | I/O | Input/output pin for testing | — | — | — | — |
| 16 | TEST1_N(*1) | I | Input pin for testing | — | — | — | — |
| 14 | RESET_N | I | Reset input pin | — | — | — | — |
| 12 | XT0 | I | Low-speed clock oscillation pin | — | — | — | — |
| 13 | XT1 | O | Low-speed clock oscillation pin | — | — | — | — |
| 59 | P00/EXI0/CAP0 | I/O | Input/output port, External interrupt 0, Capture 0 input | — | — | — | — |
| 60 | P01/EXI1/CAP1 | I/O | Input/output port, External interrupt 1, Capture 1 input | — | — | — | — |
| 61 | P02/EXI2 | I/O | Input/output port, External interrupt 2, | — | — | — | — |
| 62 | P03/EXI3 | I/O | Input/output port, External interrupt 3 | — | — | — | — |
| 63 | P04/EXI4 | I/O | Input/output port, External interrupt 4 | — | — | — | — |
| 64 | P05/EXI5 | I/O | Input/output port, External interrupt 5 | — | — | — | — |
| 1 | P06/EXI6 | I/O | Input/output port, External interrupt 6 | — | — | — | — |
| 2 | P07/EXI7 | I/O | Input/output port, External interrupt 7, | — | — | — | — |
| 49 | P20 | O | Output port | Secondary | LSCLK | O | Low-speed clock output |
| 50 | P21 | O | Output port | Secondary | OUTCLK | O | High-speed clock output |
| 51 | P40 | I/O | Input/output port | Secondary | SIN0 | I | SSIO data input |
| 52 | P41 | I/O | Input/output port | Secondary | SCK0 | I/O | SSIO synchronous clock |
| 53 | P42 | I/O | Input/output port | Secondary | SOUT0 | O | SSIO data output |
| 54 | P43 | I/O | Input/output port | — | — | — | — |
| 55 | P44/T0CK | I/O | Input/output port, Timer 0 external clock input | — | — | — | — |
| 56 | P45/T1CK | I/O | Input/output port, Timer 1 external clock input | — | — | — | — |
| 57 | P46 | I/O | Input/output port | — | — | — | — |
| 58 | P47 | I/O | Input/output port | — | — | — | — |
| 3 | PA0 | I/O | PA0 I/O Input/output port | — | — | — | — |
| 4 | PA1 | I/O | PA1 I/O Input/output port | — | — | — | — |
| 5 | PA2 | I/O | PA2 I/O Input/output port | — | — | — | — |
| 6 | PA3 | I/O | PA3 I/O Input/output port | — | — | — | — |
| 23 | COM0 | O | LCD common pin | — | — | — | — |
| 24 | COM1 | O | LCD common pin | — | — | — | — |
| 25 | COM2 | O | LCD common pin | — | — | — | — |
| 26 | COM3 | O | LCD common pin | — | — | — | — |

| PIN No. | Primary function | | | Secondary function | | | |
|---|---|---|---|---|---|---|---|
| | Pin name | I/O | Function | Secondary | Pin name | I/O | Function |
| 27 | SEG0 | O | LCD segment pin | — | — | — | — |
| 28 | SEG1 | O | LCD segment pin | — | — | — | — |
| 29 | SEG2 | O | LCD segment pin | — | — | — | — |
| 30 | SEG3 | O | LCD segment pin | — | — | — | — |
| 31 | SEG4 | O | LCD segment pin | — | — | — | — |
| 32 | SEG5 | O | LCD segment pin | — | — | — | — |
| 33 | SEG6 | O | LCD segment pin | — | — | — | — |
| 34 | SEG7 | O | LCD segment pin | — | — | — | — |
| 35 | SEG8 | O | LCD segment pin | — | — | — | — |
| 36 | SEG9 | O | LCD segment pin | — | — | — | — |
| 37 | SEG10 | O | LCD segment pin | — | — | — | — |
| 38 | SEG11 | O | LCD segment pin | — | — | — | — |
| 39 | SEG12 | O | LCD segment pin | — | — | — | — |
| 40 | SEG13 | O | LCD segment pin | — | — | — | — |
| 41 | SEG14 | O | LCD segment pin | — | — | — | — |
| 42 | SEG15 | O | LCD segment pin | — | — | — | — |
| 43 | SEG16 | O | LCD segment pin | — | — | — | — |
| 44 | SEG17 | O | LCD segment pin | — | — | — | — |
| 45 | SEG18 | O | LCD segment pin | — | — | — | — |
| 46 | SEG19 | O | LCD segment pin | — | — | — | — |
| 7 | NMI | I | non-maskable interrupt | — | — | — | — |
| 22 | NC | — | — | — | — | — | — |

(*1) Pin only for ML610Q413P

## PIN DESCRIPTION

| Pin name | I/O | Description | Primary/ Secondary | Logic |
|---|---|---|---|---|
| System | | | | |
| RESET_N | I | Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected. | — | Negative |
| XT0 | I | Crystal connection pin for low-speed clock. A 32.768 kHz crystal resonator (see measuring circuit 1) should be connected to this pin. Capacitors CDL and CGL should be connected across this pin and $V_{SS}$ . | — | — |
| XT1 | O | | — | — |
| LSCLK | O | Low-speed clock output pin. This pin is used as the secondary function of the P20 pin. | Secondary | — |
| OUTCLK | O | High-speed clock output pin. This pin is used as the secondary function of the P21 pin. | Secondary | — |
| General-purpose output port | | | | |
| P20-P21 | O | General-purpose output port.<br>Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. | Primary | Positive |
| General-purpose input/output port | | | | |
| P00-P07 | I/O | General-purpose input/output port. | Primary | Positive |
| P40-P47 | I/O | General-purpose input/output port.<br>Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. | Primary | Positive |
| PA0-PA3 | I/O | General-purpose input/output port. | Primary | Positive |

| Pin name | I/O | Description | Primary/ Secondary | Logic |
|---|---|---|---|---|
| Synchronous serial (SSIO) | | | | |
| SCK0 | I/O | Synchronous serial clock input/output pin. This pin is used as the secondary function of the P41 pin. | Secondary | — |
| SIN0 | I | Synchronous serial data input pin. This pin is used as the secondary function of the P40 pin. | Secondary | Positive |
| SOUT0 | O | Synchronous serial data output pin. This pin is used as the secondary function of the P42 pin. | Secondary | Positive |
| External interrupt | | | | |
| NMI | I | External non-maskable interrupt input pin. An interrupt is generated on both edges. | Primary | Negative |
| EXI0-7 | I | External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P07 pins. | Primary | Positive/ Negative |
| Capture | | | | |
| CAP0 | I | Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1). | Primary | Positive |
| CAP1 | I | | Primary | Positive |
| Timer | | | | |
| T0CK | I | External clock input pin used for Timer 0. The clock for this timer can be selected by software. This pin is used as the primary function of the P44 pin. | Primary | — |
| T1CK | I | External clock input pin used for Timer 1. The clock for this timer can be selected by software. This pin is used as the primary function of the P45 pin. | Primary | — |
| LCD drive signal | | | | |
| COM0-3 | O | Common output pins. | — | — |
| SEG0-19 | O | Segment output pins. | — | — |
| LCD driver power supply | | | | |
| $V_{L1}$ | — | Power supply pins for LCD bias (internally generated or positive power supply pin connected). Capacitors Ca, Cb, and Cc (see measuring circuit 1) should be connected between $V_{SS}$ and $V_{L1}$, $V_{L2}$, and $V_{L3}$, respectively. | — | — |
| $V_{L2}$ | — | | — | — |
| $V_{L3}$ | — | | — | — |
| C1 | — | Power supply pins for LCD bias (internally generated). Capacitor C12 should be connected between C1 and C2. | — | — |
| C2 | — | | — | — |
| For testing | | | | |
| TEST0 | I/O | Input/output pin for testing. A pull-down resistor is internally connected. | — | — |
| TEST1_N | I | Input pin for testing. A pull-down resistor is internally connected. This pin is only for ML610Q413P. | | |
| Power supply | | | | |
| $V_{SS}$ | — | Negative power supply pin. | — | — |
| $V_{DD}$ | — | Positive power supply pin for I/O, internal regulator, and power-on reset. | — | — |
| $V_{DDL}$ | — | Positive power supply pin (internally generated) for internal logic. Capacitor CL (see measuring circuit 1) should be connected between this pin and $V_{SS}$. | — | — |
| $V_{DDX}$ | — | Positive power supply pin (internally generated) for low-speed oscillation. Capacitor $C_X$ (see measuring circuit 1) should be connected between this pin and $V_{SS}$. | — | — |
| $V_{PP}$ | — | Power supply pin for programming Flash ROM. A pull-down resistor is internally connected. This pin is only for ML610Q413P. | — | — |

## TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

**Table 2 Termination of Unused Pins**

| Pin | Recommended pin termination |
|---|---|
| $V_{PP}$ | Open |
| $V_{L1}$, $V_{L2}$, $V_{L3}$ | Open |
| C1, C2 | Open |
| RESET_N | Open |
| TEST0 | Open |
| TEST1_N | Open |
| NMI | Open |
| P00 to P07 | Open |
| P20 to P21 | Open |
| P40 to P47 | Open |
| PA0 to PA3 | Open |
| COM0 to 3 | Open |
| SEG0 to 19 | Open |

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

($V_{SS}$ = 0V)

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage 1 | $V_{DD}$ | Ta = 25°C | –0.3 to +4.6 | V |
| Power supply voltage 2 | $V_{PP}$ | Ta = 25°C | –0.3 to +9.5 | V |
| Power supply voltage 3 | $V_{DDL}$ | Ta = 25°C | –0.3 to +3.6 | V |
| Power supply voltage 4 | $V_{DDX}$ | Ta = 25°C | –0.3 to +3.6 | V |
| Power supply voltage 5 | $V_{L1}$ | Ta = 25°C | –0.3 to +2.0 | V |
| Power supply voltage 6 | $V_{L2}$ | Ta = 25°C | –0.3 to +4.0 | V |
| Power supply voltage 7 | $V_{L3}$ | Ta = 25°C | –0.3 to +6.0 | V |
| Input voltage | $V_{IN}$ | Ta = 25°C | –0.3 to $V_{DD}$+0.3 | V |
| Output voltage | $V_{OUT}$ | Ta = 25°C | –0.3 to $V_{DD}$+0.3 | V |
| Output current 1 | $I_{OUT1}$ | Port0, Port4, PortA, Ta = 25°C | –12 to +11 | mA |
| Output current 2 | $I_{OUT2}$ | Port2, Ta = 25°C | –12 to +20 | mA |
| Power dissipation | PD | Ta = 25°C | 0.9 (TBD) | W |
| Storage temperature | $T_{STG}$ | — | –55 to +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

($V_{SS}$ = 0V)

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Operating temperature | $T_{OP}$ | | –40 to +85 | °C |
| Operating voltage | $V_{DD}$ | $f_{OP}$ = 30k to 625kHz | 2.4 to 3.6 | V |
| Operating frequency (CPU) | $f_{OP}$ | $V_{DD}$ = 2.4 to 3.6V | 30k to 625k | Hz |
| Low-speed crystal oscillation frequency*1 | $f_{XTL}$ | — | 32.768k | Hz |
| Low-speed crystal oscillation external capacitor*1 | $C_{DL}$ | — | TBD | pF |
| | $C_{GL}$ | — | TBD | |
| Capacitor externally connected to $V_{DDL}$ pin | $C_L$ | — | 0.47±30% (TBD) | µF |
| Capacitor externally connected to $V_{DDX}$ pin | $C_X$ | — | 0.1±30%(TBD) | µF |
| Capacitors externally connected to $V_{L1, 2, 3}$ pins | $C_{a, b, c}$ | — | 0.1±30% (TBD) | µF |
| Capacitors externally connected across C1 and C2 pins | $C_{12}$ | — | 0.47±30% (TBD) | µF |

*1 : Use 32.768KHz Crystal Resonator.

## OPERATING CONDITIONS OF FLASH ROM

($V_{SS}$ = 0V)

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Operating temperature | $T_{OP}$ | At write/erase | 0 to +40 | °C |
| Operating voltage | $V_{DD}$ | At write/erase*1 | 2.75 to 3.6 | V |
| | $V_{DDL}$ | At write/erase*1 | 2.5 to 2.75 | |
| | $V_{PP}$ | At write/erase*1 | 7.7 to 8.3 | |
| erase/program cycles | $C_{EP}$ | — | 80 | cycles |
| Data retention | $Y_{DR}$ | — | 10 | years |

*1: Those voltages must be supplied to $V_{DDL}$ pin and $V_{PP}$ pin when programming and erasing Flash ROM. $V_{PP}$ pin has an internal pulldown resister.

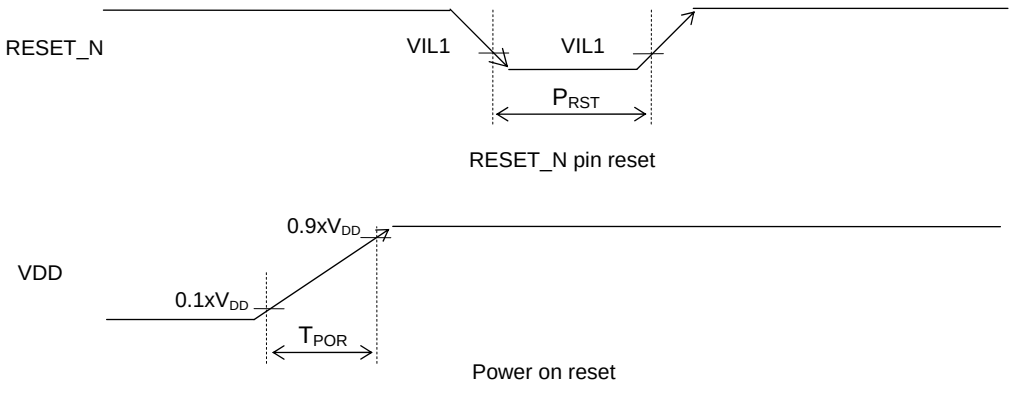
## DC CHARACTERISTICS (1/5)

($V_{DD}$ = 2.4 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | | Rating Min. | Rating Typ. | Rating Max. | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|---|
| 500kHz RC oscillation frequency | $f_{RC}$ | $V_{DD}$ = 2.4 to 3.6V | Ta = 25°C | Typ. –10% (TBD) | 500 | Typ. +10% (TBD) | kHz | 1 |
| | | | *3 | Typ. –25% (TBD) | 500 | Typ. +25% (TBD) | | |
| PLL oscillation frequency | $f_{PLL}$ | — | | -2.5% (TBD) | 8.192 | +2.5%( TBD) | MHz | |
| Low-speed crystal oscillation start time*2 | $T_{XTL}$ | — | | — | TBD | TBD | s | |
| 500kHz RC oscillation start time | $T_{RC}$ | — | | — | TBD | TBD | µs | |
| PLL oscillation start time | $T_{PLL}$ | — | | — | TBD | TBD | µs | |
| Low-speed oscillation stop detect time*1 | $T_{STOP}$ | — | | TBD | TBD | TBD | ms | |
| Reset pulse width | $P_{RST}$ | — | | 200 | — | — | µs | |
| Reset noise elimination pulse width | $P_{NRST}$ | — | | — | — | 0.3 | | |
| Power-on reset activation power rise time | $T_{POR}$ | — | | — | — | 10 | ms | |

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.
*2 : Use 32.768KHz Crystal Resonator (TBD) with capacitance $C_{GL}$=$C_{DL}$=TBD pF.
*3 : Recommended operating temperature (Ta = –40 to +85°C)

## RESET



## DC CHARACTERISTICS (2/5)

($V_{DD}$ = 2.4 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | | Rating Min. | Rating Typ. | Rating Max. | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|---|
| $V_{DDL}$ voltage | $V_{DDL}$ | $f_{OP}$ = 30k to 625kHz | | TBD | 1.2 | TBD | V | 1 |
| | | $f_{OP}$ = 4.096 MHz | | TBD | 1.7 | TBD | | |
| $V_{DDL}$ temperature deviation | $\Delta V_{DDL}$ | $V_{DD}$ = 3.0V | | — | -1 (TBD) | — | mV/°C | |
| $V_{DDL}$ voltage dependency | $\Delta V_{DDL}$ | — | | — | 5 (TBD) | 20 (TBD) | mV/V | |
| $V_{L1}$ temperature deviation | $\Delta V_{L1}$ | $V_{DD}$ = 3.0V | | — | TBD | — | mV/°C | |
| $V_{L1}$ voltage dependency | $\Delta V_{L1}$ | $V_{DD}$ = 2.4 to 3.6V | | — | TBD | TBD | mV/V | |
| $V_{L2}$ voltage | $V_{L2}$ | — | 1/2 bias | | $V_{L1}$ | | V | |
| | | | 1/3 bias | | $V_{L1}$x2 | | V | |
| $V_{L3}$ voltage | $V_{L3}$ | — | 1/2 bias | | $V_{L1}$x2 | | V | |
| | | | 1/3 bias | | $V_{L1}$x3 | | V | |
| LCD bias voltage generation time | $T_{BIAS}$ | — | | | | TBD | ms | |

## DC CHARACTERISTICS (3/5)

($V_{DD}$ = 3.0V, $V_{SS}$ = 0V, Ta = –40 to +85°C)

| Parameter | Symbol | Condition | | Rating Min. | Rating Typ. | Rating Max. | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|---|
| Supply current 1 | IDD1 | CPU: In HALT state (LTBC, WDT, RTC, Timer are Operating).*3*4 High-speed RC 500kHz oscillation: Stopped. LCD and BIAS circuits: Stopping. | Ta= 25°C | — | 1 (TBD) | TBD | μA | |
| | | | *5 | — | — | | | |
| Supply current 2 | IDD2 | CPU: In HALT state (LTBC, WDT, RTC, Timer are Operating).*3*4 High-speed RC 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. | Ta= 25°C | — | 1 (TBD) | TBD | μA | 1 |
| | | | *5 | — | — | TBD | | |
| Supply current 3 | IDD3 | CPU: In 32.768kHz operating state.*1*3 High-speed RC 500kHz oscillation: Stopped. LCD and BIAS circuits: Operating. *2 | Ta= 25°C | — | 5 (TBD) | TBD | μA | |
| | | | *5 | — | — | TBD | | |
| Supply current 4 | IDD4 | CPU: In RC 500kHz operating state. LCD and BIAS circuits: Operating. *2 | Ta= 25°C | — | 70 (TBD) | TBD | μA | 1 |
| | | | *5 | — | — | TBD | | |
| Supply current 5 | IDD5 | CPU: In 4.096 MHz operating state. LCD and BIAS circuits: Operating. *2 | Ta= 25°C | — | 950 (TBD) | TBD | μA | 1 |
| | | | *5 | — | TBD | TBD | | |

*1: When the CPU operating rate is 100% (No HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : Use 32.768KHz Crystal Resonator (TBD) with capacitance $C_{GL}$=$C_{DL}$=(TBD) pF.
*4 : Significant bits of BLKCON0/1/2/4 registers are all “1”.
*5 : Recommended operating temperature (Ta = –40 to +85°C)

## DC CHARACTERISTICS (4/5)

($V_{DD}$ = 2.4 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating Min. | Rating Typ. | Rating Max. | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| Output voltage 1 (P20, P21/ 2nd function is selected) (P00–P07) (P40–P47) (PA0–PA4) | VOH1 | IOH1 = –0.5mA, $V_{DD}$ = 2.4 to 3.6V | $V_{DD}$ –0.5 | — | — | V | 2 |
| | VOL1 | IOL1 = +0.5mA, $V_{DD}$ = 2.4 to 3.6V | —— | —— | 0.5 | | |
| Output voltage 2 (P20, P21/ 2nd function is Not selected) | VOH2 | IOH2 = –0.5mA, $V_{DD}$ = 2.4 to 3.6V | $V_{DD}$ –0.5 | — | — | | |
| | VOL2 | IOL2 = +5mA, $V_{DD}$ = 2.4 to 3.6V | — | — | 0.5 | | |
| Output voltage 4 (COM0–3) (SEG0–19) | VOH4 | IOH4 = –0.2mA, VL1=1.2V | $V_{L3}$ –TBD | — | — | | |
| | VOMH4 | IOMH4 = +0.2mA, VL1=1.2V | — | — | $V_{L2}$ +TBD | | |
| | VOMH4S | IOM4S = –0.2mA, VL1=1.2V | $V_{L2}$ –TBD | — | — | | |
| | VOML4 | IOML4 = +0.2mA, VL1=1.2V | — | — | $V_{L1}$ +TBD | | |
| | VOML4S | IOML4S = –0.2mA, VL1=1.2V | $V_{L1}$ –TBD | — | — | | |
| | VOL4 | IOL4 = +0.2mA, VL1=1.2V | — | — | TBD | | |
| Output leakage (P20, P21) (P00–P07) (P40–P47) (PA0–PA3) | IOOH | VOH = $V_{DD}$ (in high-impedance state) | — | — | 1 | µA | 3 |
| | IOOL | VOL = $V_{SS}$ (in high-impedance state) | –1 | — | — | | |
| Input current 1 (RESET_N, TEST1_N) | IIH1 | VIH1 = $V_{DD}$ | 0 | — | 1 | µA | 4 |
| | IIL1 | VIL1 = $V_{SS}$, $V_{DD}$ = 2.4 to 3.6V | TBD | TBD | TBD | | |
| Input current 1 (TEST0) | IIH1 | VIH1 = $V_{DD}$, $V_{DD}$ = 2.4 to 3.6V | TBD | TBD | TBD | | |
| | IIL1 | VIL1 = $V_{ss}$ | -1 | — | — | | |
| Input current 2 (P00-P07) (P40-P47) (PA0-PA3) | IIH2 | VIH2 = $V_{DD}$ (when pulled-down), $V_{DD}$ = 2.4 to 3.6V | TBD | TBD | TBD | | |
| | IIL2 | VIL2 = $V_{SS}$ (when pulled-up), $V_{DD}$ = 2.4 to 3.6V | TBD | TBD | TBD | | |
| | IIH2Z | VIH2 = $V_{DD}$ (in high-impedance state) | — | — | 1 | | |
| | IIL2Z | VIL2 = $V_{SS}$ (in high-impedance state) | –1 | — | — | | |

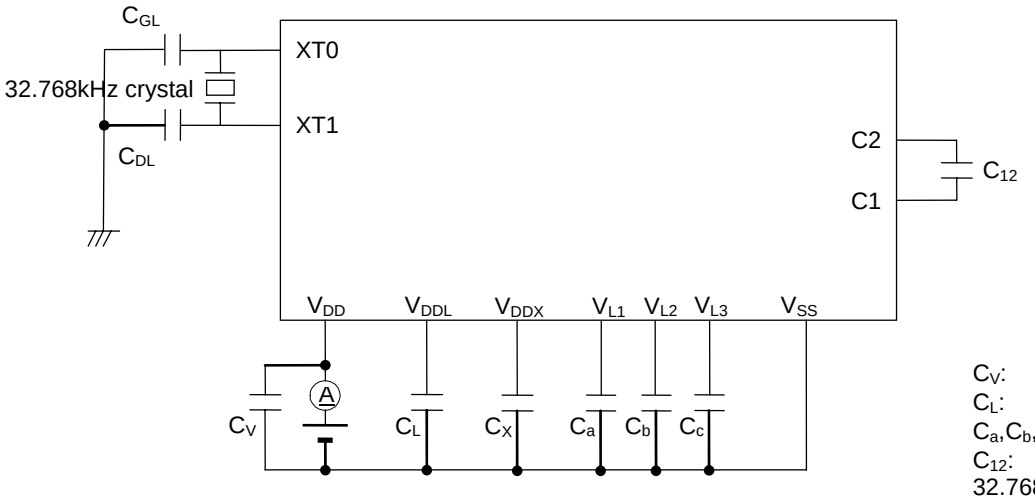
## DC CHARACTERISTICS (5/5))

($V_{DD}$ = 2.4 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input voltage 1 (RESET_N) (TEST0, TEST1_N) (P00–P07) (P40–P47) (PA0–PA3) | VIH1 | $V_{DD}$ = 2.4 to 3.6V | 0.7 ×$V_{DD}$ (TBD) | — | $V_{DD}$ | V | 5 |
| | VIL1 | $V_{DD}$ = 2.4 to 3.6V | 0 | — | 0.3 ×$V_{DD}$ (TBD) | | |
| Input pin capacitance (P00–P07) (P40–P47) (PA0–PA3) | CIN | f = 10kHz<br>$V_{rms}$ = 50mV<br>Ta = 25°C | — | — | 5 | pF | — |

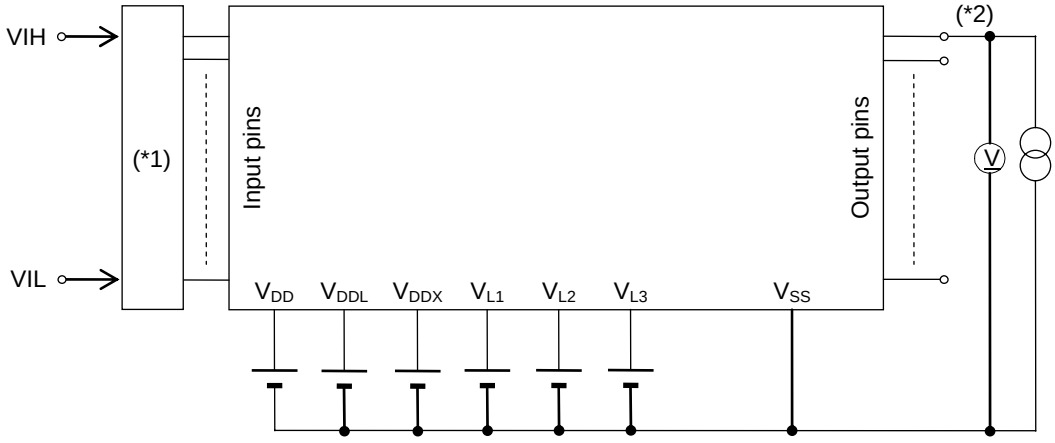
## MEASURING CIRCUITS

### MEASURING CIRCUIT 1 (TBD)



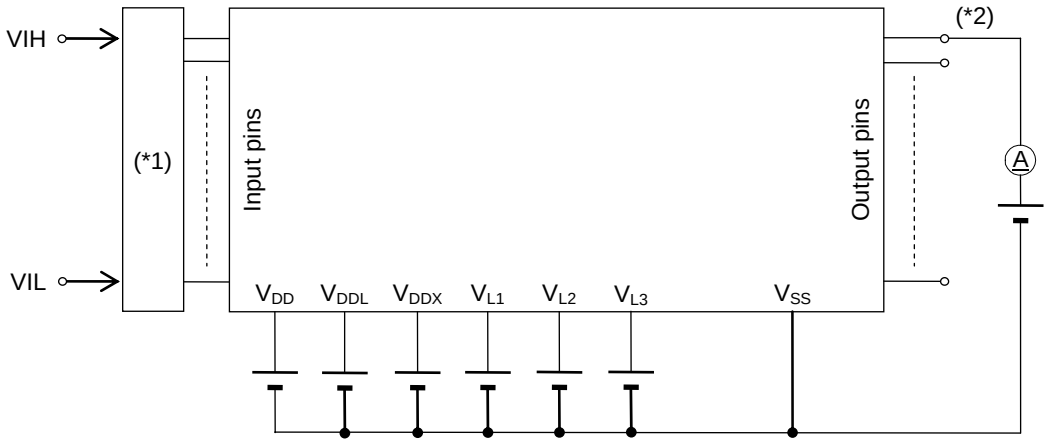

| | |
|---|---|
| $C_V$: | 1µF |
| $C_L$: | 0.47µF |
| $C_a$,$C_b$,$C_c$,$C_X$: | 0.1µF |
| $C_{12}$: | 0.47µF |
| 32.768kHz crystal: | (TBD) |
| $C_{GL}$, $C_{DL}$: | TBD |

### MEASURING CIRCUIT 2 (TBD)



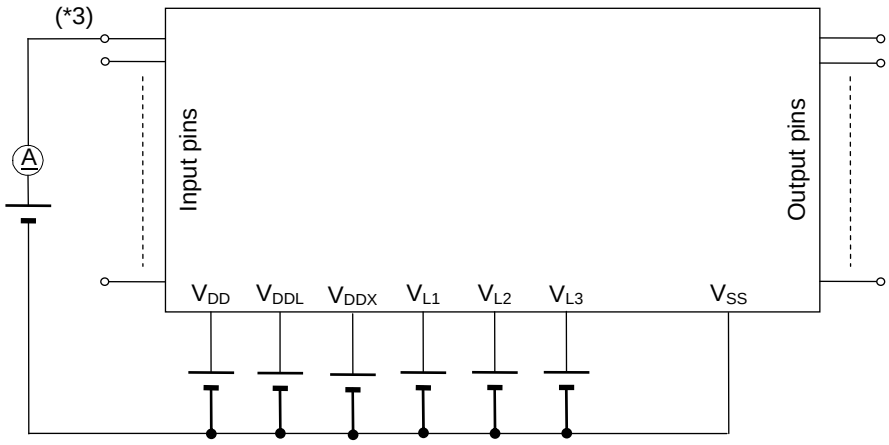

(*1): Input logic circuit to determine the specified measuring conditions.
(*2): Measured at the specified output pins.

## MEASURING CIRCUIT 3 (TBD)



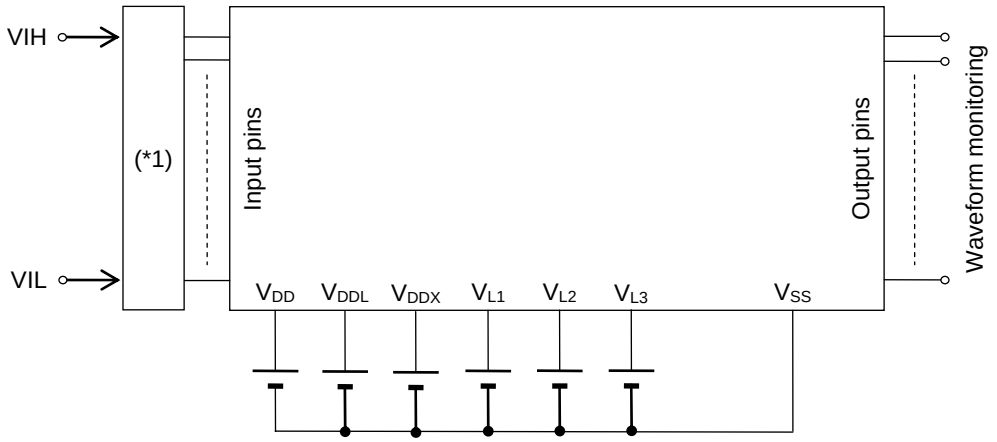

(*1): Input logic circuit to determine the specified measuring conditions.
(*2): Measured at the specified output pins.

## MEASURING CIRCUIT 4 (TBD)




(*3): Measured at the specified output pins.

## MEASURING CIRCUIT 5 (TBD)

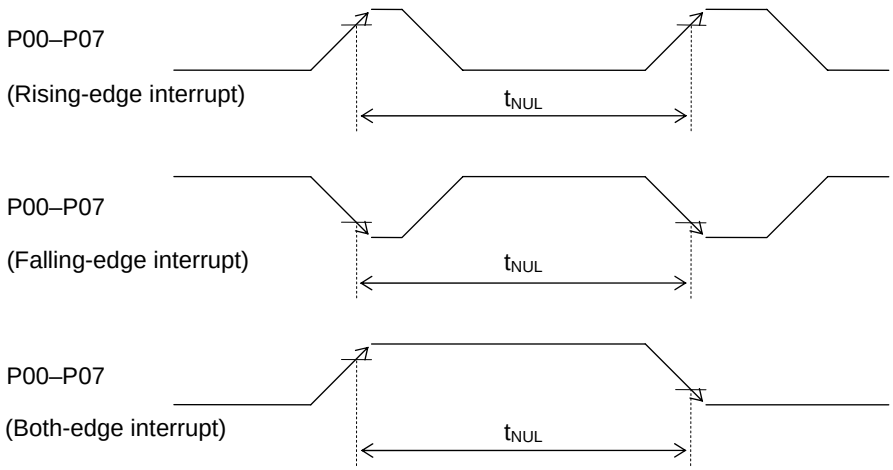



(*1): Input logic circuit to determine the specified measuring conditions.

## AC CHARACTERISTICS (External Interrupt)

($V_{DD}$ = 2.4 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| External interrupt disable period | $T_{NUL}$ | Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz | 76.8 | — | 106.8 | µs |
| Minimum NMI interrupt pulse width | $T_{NMI}$ | — | — | — | TBD | ns |

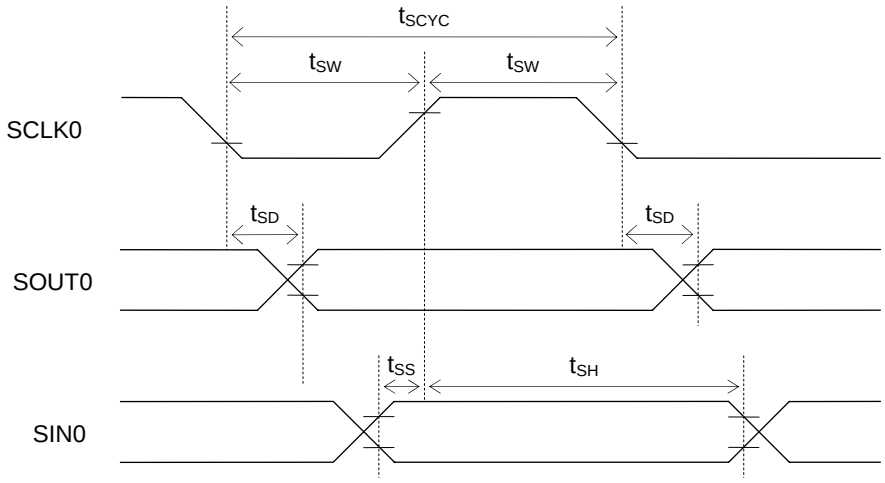


## AC CHARACTERISTICS (Synchronous Serial Port)

($V_{DD}$ = 2.4 to 3.6V, $V_{SS}$ = 0V, Ta = –40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| SCLK0 input cycle (slave mode) | $t_{SCYC}$ | When RC oscillation is 500kHz *2 ($V_{DD}$ = 2.4 to 3.6V) | 10 | — | — | µs |
| SCLK0 output cycle (master mode) | $t_{SCYC}$ | — | — | SCLK0*1 | — | µs |
| SCLK0 input pulse width (slave mode) | $t_{SW}$ | When RC oscillation is 500kHz *2 ($V_{DD}$ = 2.4 to 3.6V) | 4 | — | — | µs |
| SCLK0 output pulse width (master mode) | $t_{SW}$ | — | SCLK0*1 ×0.4 | SCLK0*1 ×0.5 | SCLK0*1 ×0.6 | s |
| SOUT0 output delay time (slave mode) | $t_{SD}$ | When RC oscillation is 500kHz *2 ($V_{DD}$ = 2.4 to 3.6V) output load 10pF | — | — | 500 | ns |
| SOUT0 output delay time (master mode) | $t_{SD}$ | When RC oscillation is 500kHz *2 ($V_{DD}$ = 2.4 to 3.6V) output load 10pF | — | — | 500 | ns |
| SIN0 input setup time (slave mode) | $t_{SS}$ | — | 80 | — | — | ns |
| SIN0 input setup time (master mode) | $t_{SS}$ | When RC oscillation is 500kHz *2 ($V_{DD}$ = 2.4 to 3.6V) | 500 | — | — | ns |
| SIN0 input hold time | $t_{SH}$ | When RC oscillation is 500kHz *2 ($V_{DD}$ = 2.4 to 3.6V) | 300 | — | — | ns |

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)
*2: When RC oscillation is selected with OSCM1 and OSCM0 of the frequency control register (FCON0)




*: Indicates the secondary function of the port

## REVISION HISTORY

| Document No. | Date | Page | | Description |
|---|---|---|---|---|
| | | Previous Edition | Current Edition | |
| PEDL610413-01 | Mar.12,2010 | – | – | Preliminary edition 1 |
| PEDL610413-02 | Apr.13,2010 | 1<br>2 | 1<br>2 | Add 4.096 MHz system clock.<br>Add Disable function(WDT). |
| PEDL610413-03 | Jun. 10, 2010 | – | – | Preliminary edition 3 |
| | | 1 | 1 | Remove 4.096 MHz system clock.<br>Change the size of the internal RAM to 512bytes.<br>Add a description of the FLASH ROM model.<br>Remove interrupt sources from LTBC.<br>Remove 1 hour interrupt of RTC. |
| | | 2 | 2 | Modify the description of WDT.<br>Modify the description of reset.<br>Add 1/2 bias of LCD driver. |
| | | 3 | 3 | Add a description of Security Mesh.<br>Add 64pin TQFP. |
| | | – | 4 | Add the block diagram of the FLASH ROM model. |
| | | – | 6 | Add the pin layout of 64pin TQFP. |
| | | 7 | 9 | Change P00-P07 to “input/output”. |
| | | 9 | 11 | Change P00-P07 to “input/output”. |
| | | 10 | 12 | Remove “battery low detector”. |
| | | 20 | – | Remove APPENDIX. |
| PEDL610413-04 | Jul. 7, 2010 | 1 | 1 | The Security Mesh interrupt is added. |
| | | 2 | 2 | The SSIO overflow detection is added<br>The frame frequency 16Hz is added, 102Hz is deleted.<br>The contrast adjustment function is added |
| | | 3 | 3 | The built-in PLL is added. ( 4MHz clock selectable )<br>In the Security Mesh, the interrupt or the reset is selectable. |
| | | 4 | 4 | The Security Mesh interrupt is added.<br>The $V_{DDX}$ terminal is added |
| | | 5 | 5 | The Security Mesh interrupt is added.<br>The $V_{DDX}$ terminal is added |
| | | 9 | 9 | The $V_{DDX}$ terminal is added |
| | | 12 | 12 | The $V_{DDX}$ terminal is added |
| PEDL610413-05 | Jul. 20, 2010 | 2 | 2 | The contrast adjustment is deleted. |
| | | 7 | 7 | The PAD aperture is changed to 70 μm × 80 μm |
| | | 14 | 14 | The $C_a$, $C_b$, $C_c$, and $C_{12}$ are changed to 1.0 μF. |
| PEDL610413-06 | Aug. 20, 2010 | 9 | 9 | The “PIN No” are decided. |
| | | – | – | The product name is changed.<br>ML610413 -> ML610413P<br>ML610Q413-> ML610Q413P |
| | | 14 | 14 | The $C_a$, $C_b$, $C_c$ are changed to 0.1 uF.<br>The $C_{12}$ is changed to 0.47 μF. |

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

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